a debug circuit, wherein the processor and debug circuit are implemented on a same integrated circuit;

a system bus coupling the processor and debug circuit; and

a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a program counter value indicating the program counter of the processor.

3. (Amended) The microcomputer according to claim 2, wherein the processor is further configured to transmit to the debug circuit a status indicating that a computer instruction is in the writeback stage is a valid computer instruction.

4. (Amended) The microcomputer according to claim 3, wherein the processor is further configured to transmit to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

5. (Amended) The microcomputer according to claim 1, wherein the processor is further configured to transmit to the debug circuit a value indicating an increment of the program counter of the processor.

7. (Amended) The microcomputer according to claim 1, wherein the processor is further configured to transmit to the debug circuit a signal indicating that a current process identifier value differs from a process identifier value of a previously-executed instruction.

Please cancel claim 10 without prejudice or disclaimer.

12. (Amended) A microcomputer comprising:

at least one processor;

a debug circuit, wherein the processor and debug circuit are implemented on a same integrated circuit;

a system bus coupling the processor and debug circuit; and